UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/432,927	11/03/1999	JUNJI NISHIGAKI	15162/01250	1794

24367 7590 04/17/2006

SIDLEY AUSTIN LLP
717 NORTH HARWOOD
SUITE 3400
DALLAS, TX 75201

EXAMINER	
GRANT II, JEROME	
ART UNIT	PAPER NUMBER
2625	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/432,927	NISHIGAKI, JUNJI	
	Examiner	Art Unit	
	Jerome Grant II	2626	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7 and 9-12* is/are rejected.

7)☒ Claim(s) *3, 6, 8 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4, 5 and 9-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Katsurabayashi (5,996,002).

With respect to claim 1, Katsurabayashi teaches an image processing apparatus (as shown by figure 1), comprising: synchronous type processing means 9computers 2b, 2c and 2d) for carrying out a first image process on image data (image data across the network 1) that is the subject of processing (data shared on common screen (CW)); asynchronous type processing means 2a for carrying out a second image

(hand written notes by user) process on image data of a region of said image data that is the subject of processing (CW); and synthesized means (page creation 22 and data manager 16) for synthesizing an output of said synchronous type processing means and an output of said asynchronous type processing means to form one image data, See also col. 9, lines 30-33.

With respect to claim 2, Katsurabayashi teaches wherein the synthesize means comprises: a memory (data memory 14 and 15) in which an output of said synchronous type processing means is stored, and replacement means (data manager 16 and input section 12) for replacing a portion of an output of said synchronous type processing means stored in said memory with an output of said synchronous type processing means."

With respect to claim 4, Katsurabayashi teaches an image processing apparatus, shown by figure 1, comprising: a first image processor 2b, 2c, 2d of a hardware circuit (computers 2b-2d) for carrying out a first image process on the input image data; a second image processor 2a carrying out a second image process on a fragment (layer, col. 7, lines 35-41 and 48-53) of said input image data according to a program of predetermined software (col. 8, lines 36-40); and a memory 14, 15 in which image data subjected to said first image process and image data subjected to said second image process are synthesized and stored. See col. 9, lines 28-36.

With respect to claim 5, Katsurabayshi teaches wherein data of said memory in which image data subjected to the first image process is stored is overwritten (in that the user data is written in exchange of a predetermined area of where synchronous data was first stored) by the image data subjected to the second image prodess. See col. 8, lines 57-62.

With respect to claim 9, Katsurabayshi teaches an image processing method comprising the steps of:

Carrying out a first image process (computer 2b-2d) on input image data through hardware circuit (computer hardware); carrying out a second iamge process (computer 2a) on a fragment (layer according to col. 7, lines 35-41 and 48-53) of the input image data through software (col. 8, lines 36-40); and synthesized means (page creation 22 and data manager 16) for synthesizing image data subjected to the first and second processes, see also col. 9, lines 30-33; wherein sequence of said first and second image processes is arbitrary (because it is based on users at 2b-2d) entering the user data) or alternatively not deciding to enter the user data arbitrarily.

With respect to claim 10, Katsurabayashi teaches the step of detecting a region (layer area) on which the second image process is to be carried out (user input data) and carrying out the second image process o the detected region (layer area). See col. 7, lines 38-43 and 48-55.

With respect to claim 11, Katsurabayashi teaches an image processing apparatus shown by figure 1, an image processing system (as shown by figure 1), comprising: synchronous type processing means (computers 2b, 2c and 2d) for carrying out a first image process on image data (image data across the network 1) that is the subject of processing (data shared on common screen (CW)); asynchronous type processing means 2a for carrying out a second image (hand written notes by user) process on image data of a predetermined region of said image data that is the subject of processing (CW); and data synthesizing device (data manager 16 and input section 12) for synthesizing an output of said synchronous type processing means and an output of said asynchronous type processing means to form one image data, see also col. 9, lines 30-33.

With respect to claim 12, Katsurabayashi teaches wherein the synthesize means comprises: a memory (data memory 14 and 15) in which an output of said synchronous type processing means is stored, and replacement means (data manager 16 and input section 12) for replacing a portion of an output of said synchronous type processing means stored in said memory with an output of said synchronous type processing means."

2

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Katsurabayashi.

Katsurabayashi teaches the use of a program that is stored as software, see col. 8, lines 36-40. However, it cannot be determined from the reference whether the program is specifically rewritable. Hence, it seems as a matter of reasonable intelligence that a program can be written, for example to account for misspellings or to add to it subroutines that perform additional functions or programs in addition to what was originally written. Such programs may be stored, as a matter of skill in the art, on EEPROMS which are programmable memories. Hence a program could be edited if stored by an EEPROM. Therefore, one of ordinary skill in the art would have known to store programs that could be rewritten on a computer readable medium such as an EEPROM or any other known equivalent memory space for storing computer programs.

3

Claims Objected as Containing Allowable Matter

Claims 3, 6, 8 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. **Examiner's Comments**

In the first full paragraph of page 1, at page 6, applicant argues that Katsurabayashi does not disclose the structure recited in claim1. Inference is made regarding the first two processors. The examiner strongly disagrees with applicant's contention. Applicant fails to show why elements 2b, 2c and 2d as the first processing means and processor 2a as the second processing means, fails to teach the claimed limitations. Applicant's arguments appear to be only allegations.

With respect to the second full paragraph of page 6, applicant argues that Katsurabayashi does not provide information as to how layers are combined. Upon

closer view, there is no language in claim 1 directed toward layers or how they are combined. Applicant is arguing limitations which are not support in the claim.

Regarding the third full paragraph of page 6, applicant contends that plural computers do not comprise an apparatus. Why does applicant believe this ? What proof has applicant provided that clearly defines a plurality of computers is precluded from being identified as being in an apparatus or comprising one.

Regarding the fourth limitation of the claim this contention appears only to be an allegation. No proof has been provided. Applicant has clearly delineated the elements which comprise the asynchronous and synchronous processor. No evidence has been proffered to the contrary.

In the third full paragraph of page 7, applicant argues that an image processing apparatus is not provided by Katsurabayashi. The examiner contends that sufficient evidence to the contrary has been provided by the examiner and that applicant has made allegations of limitations not taught without support for the position taken.

5.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jerome Grant II whose telephone number is 571-272-7463. The examiner can normally be reached on Mon.-Thurs. from 9:00 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Moore, can be reached on 571-272-7437. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J. Grant II